KAKATIYA INSTITUTE OF TECHNOLOGY AND SCIENCE: WARANGAL – 15

DEPARTMENT OF ELECTRONICS & INSTRUMENTATION ENGINEERING

M.TECH (VLSI & EMBEDDED SYSTEM) (II-Semester) Class work Time Table (2015-16)

Class Teacher: Sri O.Anjaneyulu Room No. B IV 001 A w.e.f. 25.01.2016

Day / Time	9.40 - 10.30	10.30 -11.20	11.20 -12.10	12.10 - 1.00		2.00 - 2.50	2.50 - 3.40	3.40 - 4.30
Monday	ACSA	MSD	ASICD	RTOS	L	←------LAB DUTY----------→		
Tuesday	LPVLSI	←---ESD LAB--------→ KSJ			U	ASICD	HSD	HSD
Wednesday	HSD	LPVLSI	MSD	ASICD	N	RTOS	ACSA	-
Thursday	RTOS	ACSA	MSD	LPVLSI	C	←----MSD LAB---------→ OA		
Friday	ACSA	HSD	RTOS	ASICD	H	MSD	LPVLSI	--
Saturday								

MSD	:	Mixed Signal Design	:	Sri O.Anjaneyulu(OA)
LPVLSI	:	Low Power VLSI	:	Sri B.Jeevan(BJ)
ACSA	:	Advanced Computer System Architecture	:	Md.Abdul Muqueem (MQ)
ASICD	:	ASIC Design	:	Sri G.Raju (GR)
RTOS	:	RTOS for Embedded Systems	:	Smt K.Shailaja (KSJ)
HSD	:	Hardware-Software Co-Design	:	Sri B.Krishna Sundeep(BKS)
ESD LAB	:	Embedded System Design LAB	:	Smt K.Shailaja(KSJ)
MSD LAB	:	Mixed Signal Design LAB	:	Sri O.Anjaneyulu

I/c Time Table (Smt B.Smitha

Coordinator (Time Tables) Dr.M.Andal

HoD, Dept. of E&I (Prof.M.Sreelatha)

Dean, Academic Affairs (Prof.R.Ravinder Rao)

PRINCIPAL (Dr.K.GURU RAJ)