KAKATIYA UNIVERSITY: WARANGAL

TIME TABLE M.TECH I Year I SEMESTER EXAMINATION

CENTRE: *KAKATIYA INSTITUTE OF TECHNOLOGY AND SCIENCE, WARANGAL.*

a) Kakatiya Institute of Technology and Science, Warangal b) Warangal Institute of Technology & Science, Oorugonda, Warangal
c) Chaitanya Institute of Technology & Science, Madikonda, Warangal d) Vinuthna Institute of Technology & Science, Hasanparthy
e) KU College of Engineering & Technology, KU Campus

TIME:: 10.30 am to 01.30 pm

Date & Day	Structural & Construction Engineering	Design Engineering & CAD/CAM	Digital Communication	Software Engineering	Computer Science and Engineering	VLSI & Embedded System Design and VLSI Systems Design	Power Electronics
17-02-2014 Monday	Numerical and Statistical Methods	Optimization Methods in Engineering Design (Common to DE & CAD/CAM)	Detection & Estimation Theory	Discrete Mathematics & Optimization Techniques	Data Structures and Algorithms Design	Optimization Techniques & Graph Theory (VLSI & Embedded System Design Only) Advanced Digital Signal Processing (VLSI Systems Design Only)	Machine Modeling & Analysis
18-02-2014 Tuesday	Limit Analysis of Concrete Structures	Fundamental Principles of Engineering Design(Common to DE & CAD/CAM)	Data & Computer Communication	Object Oriented Software Engineering	Advanced Software Engineering	Digital Design (Common VLSI & Embedded System Design and VLSI system Design)	Analysis of Power Electronic Converts
19-02-2014 Wednesday	Advanced Concrete Technology	Stress Analysis (Common to DE & CAD/CAM)	Advanced Digital Signal Processing	Software Project Management	Computer Networks and Security	Analog Design (Common VLSI & Embedded System Design and VLSI system Design)	Modern Control Theory
20-02-2014 Thursday	Advanced Analysis of Structures	Mechanical Vibrations (Common to DE & CAD/CAM)	Microwave & Optical Fiber Communication System	Advanced Operating Systems	Data Mining & Data Warehousing	VLSI Technology (Common VLSI & Embedded System Design and VLSI system Design)	Power Electronic Controls of DC Drives
21-02-2014 Friday	Construction Techniques and Equipment	Computer Aided Design & Graphics (Common to DE & CAD/CAM)	Data Compression Techniques	Advanced Computer Architecture	Advanced Computer Architecture	Embedded Systems Concepts (Common VLSI & Embedded System Design and VLSI system Design)	Elective - I HVDC Transmissions
22-02-2014 Saturday	**ELECTIVE - I** Total Quality Management	**ELECTIVE - I (d) Smart Structures** (DE Only) a) Fault Diagnosis of Machines (CAD/CAM Only)	**ELECTIVE - Embedded System Design** Artificial Neural Network	**ELECTIVE - I** (a) Data Structures & Algorithms (d) Genetic Algorithms	**Elective - I Advances in Compiler Construction**	**ELECTIVE - I** Data Communication & Computer Networks (Common VLSI & Embedded System Design and VLSI system Design)	Elective - II Alternative Sources of Electronic Energy

CONTROLLER OF EXAMINATIONS

Note: - *Any Omission or Clash in the Time-Table may kindly be intimated to the Controller of Examination, K.U., Warangal, immediately.*